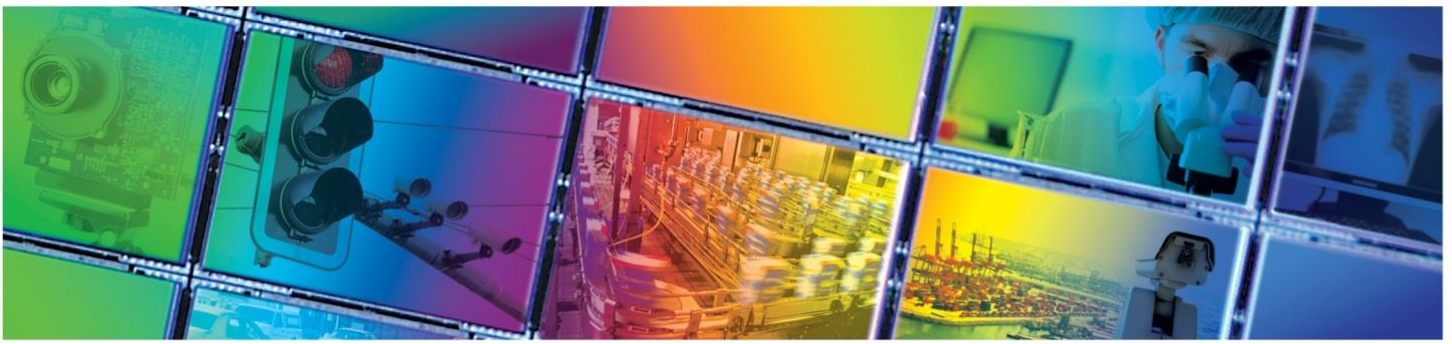


**ON Semiconductor®**



**KAI-16000 IMAGE SENSOR**  
**4872 (H) X 3248 (V) INTERLINE CCD IMAGE SENSOR**



**JUNE 4, 2014**  
**DEVICE PERFORMANCE SPECIFICATION**  
**REVISION 3.1 PS-0013**



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## Summary Specification

### KAI-16000 Image Sensor

#### DESCRIPTION

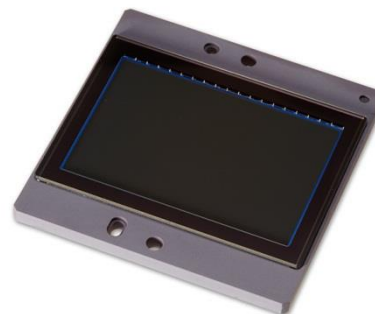
The KAI-16000 is an interline transfer CCD offering 16 million pixels at up to 3 frames per second through 2 outputs. This image sensor is organized into an array of 4,872 (H) x 3,248 (V) with 7.4 micron square pixels and full 35mm optical format. As an interline transfer CCD, the KAI-16000 includes additional features such as progressive scan readout, electronic shutter, low noise, high dynamic range, and blooming suppression. These features make the KAI-16000 the perfect sensor for applications in Industrial, Aerial, Security, and Scientific markets.

#### FEATURES

- 16 Million pixel resolution
- Electronic shutter
- 35mm Optical format
- Progressive scan readout
- High sensitivity
- Fast Frame rate
- >60 dB dynamic range

#### APPLICATIONS

- Industrial
- Aerial Photography
- Security
- Scientific



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	4960 (H) x 3324 (V) = 16.6M
Number of Effective Pixels	4904 (H) x 3280 (V) = 16.1M
Number of Active Pixels	4872 (H) x 3248 (V) = 15.8M
Pixel Size	7.4 $\mu\text{m}$ (H) x 7.4 $\mu\text{m}$ (V)
Active Image Size	36.1 mm (H) x 24.0 mm (H) 43.3 mm (diagonal)
Aspect Ratio	3:2
Number of Outputs	1 or 2
Saturation Signal	30,000 electrons
Output Sensitivity	30 $\mu\text{V}/\text{e}$
Quantum Efficiency KAI-16000-AXA (500nm)	45%
Quantum Efficiency KAI-16000-CXA R(630nm), G(540nm), B(470nm)	30%, 37%, 42%
Read Noise (f=30MHz)	16 electrons
Dark Current	< 0.5 nA/cm <sup>2</sup>
Dark Current Doubling Temperature	7 °C
Dynamic Range	65 dB
Charge Transfer Efficiency	0.99999
Blooming Suppression	> 100X
Smear	< -80 dB
Image Lag	< 10 electrons
Maximum Data Rate	30 MHz per channel
Package	40 pin Grid Array
Cover Glass	AR coated, 2 sides

All parameters above are specified at T = 40 °C



## Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0856	KAI-16000-AAA-JR-B1	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 1	KAI-16000-AAA (Serial Number)
4H0857	KAI-16000-AAA-JR-B2	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 2	
4H0858	KAI-16000-AAA-JR-AE	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Engineering Grade	
4H2001	KAI-16000-AAA-JD-B1	Monochrome, No Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (2 sides), Grade 1	
4H2002	KAI-16000-AAA-JD-B2	Monochrome, No Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (2 sides), Grade 2	
4H2003	KAI-16000-AAA-JD-AE	Monochrome, No Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (2 sides), Engineering Grade	
4H2226	KAI-16000-AXA-JD-BX	Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Special Grade	KAI-16000-AXA (Serial Number)
4H0850	KAI-16000-AXA-JD-B1	Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 1	
4H0851	KAI-16000-AXA-JD-B2	Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 2	
4H0852	KAI-16000-AXA-JD-AE	Monochrome, Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2109	KAI-16000-AXA-JR-B1	Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 1	
4H2110	KAI-16000-AXA-JR-B2	Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Grade 2	
4H2111	KAI-16000-AXA-JR-AE	Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (2 sides), Engineering Grade	KAI-16000-CXA (Serial Number)
4H0853	KAI-16000-CXA-JD-B1	Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 1	
4H0854	KAI-16000-CXA-JD-B2	Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Grade 2	
4H0855	KAI-16000-CXA-JD-AE	Color (Bayer RGB), Special Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Grade	

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.truesenseimaging.com](http://www.truesenseimaging.com).

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.  
1964 Lake Avenue  
Rochester, New York 14615

Phone: (585) 784-5500  
E-mail: [info@truesenseimaging.com](mailto:info@truesenseimaging.com)

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## Device Description

### ARCHITECTURE

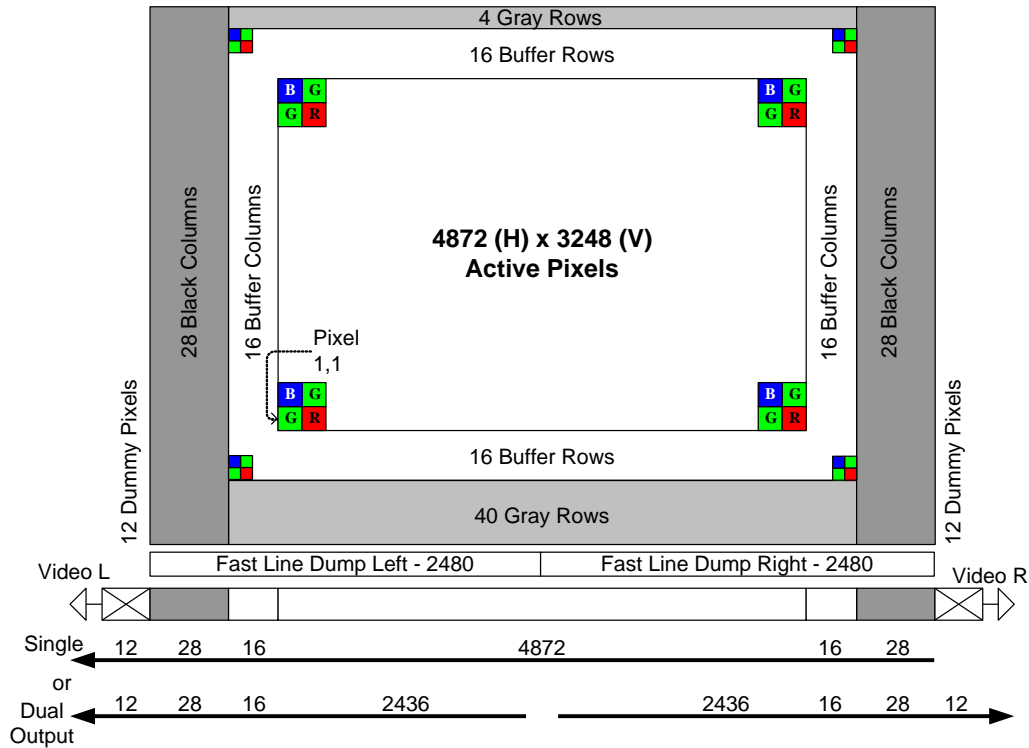


Figure 1: Sensor Architecture

There are 40 light shielded gray rows followed 3280 photoactive rows and finally 4 more light shielded gray rows. The first 16 and the last 16 photoactive rows are buffer rows giving a total of 3248 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 12 empty pixels of each line do not receive charge from the vertical shift register. The next 28 pixels receive charge from the left light shielded edge followed by 4904 photosensitive pixels and finally 28 more light shielded pixels from the right edge of the sensor. The first 16 and last 16 photosensitive pixels are buffer pixels giving a total of 4872 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. For the Video L each row consists of 12 empty pixels followed by 28 light shielded pixels followed by 2452 photosensitive pixels. For the Video R each row consists of 12 empty pixels followed by 28 light shielded pixels followed by 2452 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

The gray rows are not entirely dark and so should not be used for a dark reference level. Use the dark columns on the left or right side of the image sensor as a dark reference.

Of the dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns.



## PIN DESCRIPTION AND PHYSICAL ORIENTATION

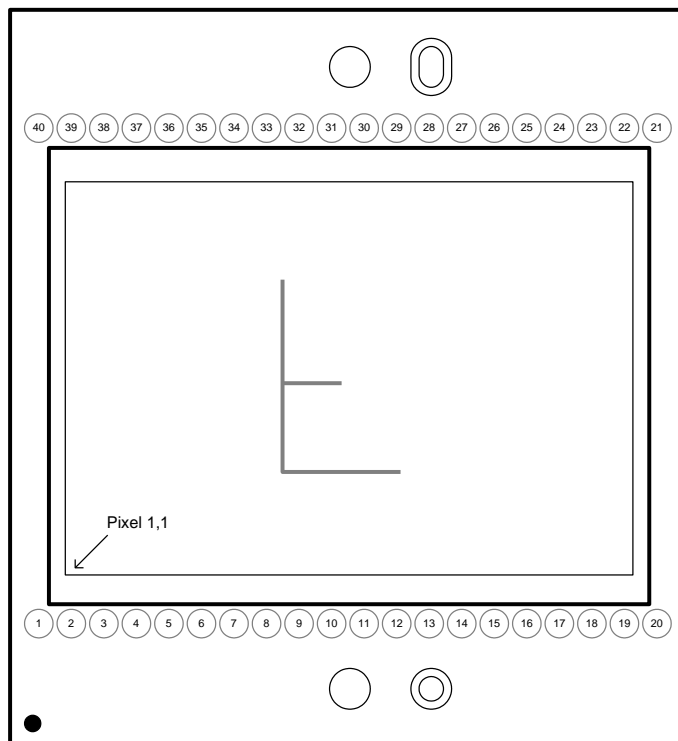


Figure 2: Package Pin Designations - Top View

Pin	Name	Description
1	VOUTL	Video Output, Left
2	VDDL	Vdd, Left
3	GND	Ground
4	RESETL	Reset Gate, Left
5	HLASTL	Horizontal Clock, Last Stage, Left
6	H2BL	Horizontal Clock, Phase 2, Barrier, Left
7	H1BL	Horizontal Clock, Phase 1, Barrier, Left
8	H1SL	Horizontal Clock, Phase 1, Storage, Left
9	H2SL	Horizontal Clock, Phase 2, Storage, Left
10	ESD	ESD Protection Disable
11	GND	Ground
12	H2SR	Horizontal Clock, Phase 2, Storage, Right
13	H1SR	Horizontal Clock, Phase 1, Storage, Right
14	H1BR	Horizontal Clock, Phase 1, Barrier, Right
15	H2BR	Horizontal Clock, Phase 2, Barrier, Right
16	HLASTR	Horizontal Clock, Last Stage, Right
17	RESETR	Reset Gate, Right
18	GND	Ground
19	VDDR	Vdd, Right
20	VOUTR	Video Output, Right

Pin	Name	Description
40	FDGL	Fast Line Dump Gate, Left
39	RDL	Reset Drain, Left
38	SUB	Substrate
37	GND	Ground
36	V1	VCCD Gate 1, Phase 2
35	V5	VCCD Gate 5, Phase 2
34	V9	VCCD Gate 9, Phase 2
33	V3	VCCD Gate 3, Phase 2
32	V7	VCCD Gate 7, Phase 2
31	V11	VCCD Gate 11, Phase 2
30	V2	VCCD Gate 2, Phase 1
29	V6	VCCD Gate 6, Phase 1
28	V10	VCCD Gate 10, Phase 1
27	V4	VCCD Gate 4, Phase 1
26	V8	VCCD Gate 8, Phase 1
25	V12	VCCD Gate 12, Phase 1
24	GND	Ground
23	SUB	Substrate
22	RDR	Reset Drain, Right
21	FDGR	Fast Line Dump Gate, Right





## Imaging Performance

### TYPICAL OPERATIONAL CONDITIONS

Unless otherwise noted, the Specifications are measured using the following conditions.

Description	Condition	Notes
Frame Time	908 msec	1
Horizontal Clock Frequency	20 MHz	
Light Source	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2,3
Operation	Nominal operating voltages and timing	

#### Notes:

1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

### SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Temperature Tested At (°C)	Notes	Sample Plan <sup>7</sup>
Global Non-Uniformity		n/a	2.5	5.0	%rms	27, 40	1	Die
Maximum Photoresponse Nonlinearity	NL	n/a	2		%		2, 3	Design
Maximum Gain Difference Between Outputs	$\Delta G$	n/a	10		%		2, 3	Design
Max. Signal Error due to Nonlinearity Dif.	$\Delta NL$	n/a	1		%		2, 3	Design
Horizontal CCD Charge Capacity	HNe		100		ke <sup>-</sup>			Design
Vertical CCD Charge Capacity	VNe		50		ke <sup>-</sup>	27, 40		Die
Photodiode Charge Capacity	PNe	28	30		ke <sup>-</sup>	27, 40	4	Die
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999		n/a				Design
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999		n/a				Design
Photodiode Dark Current	l <sub>pd</sub>	n/a	40	350	e/p/s	40		Die
Photodiode Dark Current	l <sub>pd</sub>	n/a	0.01	0.1	nA/cm <sup>2</sup>	40		Die
Vertical CCD Dark Current	l <sub>vd</sub>	n/a	400	1711	e/p/s	40		Die
Vertical CCD Dark Current	l <sub>vd</sub>	n/a	0.12	0.5	nA/cm <sup>2</sup>	40		Die
Dark Current Doubling Temperature	$\Delta T$	n/a	7	n/a	°C			Design
Image Lag	Lag	n/a	<10	50	e <sup>-</sup>			Design
Antiblooming Factor	X <sub>ab</sub>	100	300	n/a				Design
Vertical Smear	Smr	n/a	-80	-75	dB			Design
Read Noise	n <sub>e-T</sub>		16		e <sup>-</sup> rms		5	Design
Dynamic Range	DR		65		dB		5, 6	Design
Output Amplifier DC Offset	V <sub>odc</sub>	4	9.5	14	V	27, 40		Die
Output Amplifier Bandwidth	F <sub>-3db</sub>		140		MHz			Design
Output Amplifier Impedance	R <sub>OUT</sub>	100	130	200	Ohms	27, 40		Die
Output Amplifier Sensitivity	$\Delta V/\Delta N$		30		μV/e <sup>-</sup>			Design



### KAI-16000-AAA

Description	Symbol	Min.	Nom.	Max.	Units	Temperature Tested At (°C)	Notes	Sample Plan <sup>7</sup>
Peak Quantum Efficiency	QE <sub>max</sub>		11	n/a	%			Design
Peak Quantum Efficiency Wavelength	λQE	n/a	500	n/a	nm			Design

### KAI-16000-AXA

Description	Symbol	Min.	Nom.	Max.	Units	Temperature Tested At (°C)	Notes	Sample Plan <sup>7</sup>
Peak Quantum Efficiency	QE <sub>max</sub>		45	n/a	%			Design
Peak Quantum Efficiency Wavelength	λQE	n/a	500	n/a	nm			Design

### KAI-16000-CXA

Description	Symbol	Min.	Nom.	Max.	Units	Temperature Tested At (°C)	Notes	Sample Plan <sup>7</sup>
Peak Quantum Efficiency	QE <sub>max</sub>		42	n/a	%			Design
Blue			37	n/a				
Green			30	n/a				
Peak Quantum Efficiency Wavelength	λQE	n/a	470	n/a	nm			Design
Blue		n/a	540	n/a				
Green		n/a	630	n/a				

n/a: not applicable

#### Notes:

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning
4. The operating of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of Vab is set such that the photodiode charge capacity is 30,000 electrons.
5. At 30 MHz
6. Uses 20LOG(PNe/ n<sub>e-T</sub>)
7. "Die" indicates a parameter that is measured on every sensor during the production testing. "Design" designates a parameter that is quantified during the design verification activity.



## Typical Performance Curves

### MONOCHROME WITH MICROLENS QUANTUM EFFICIENCY

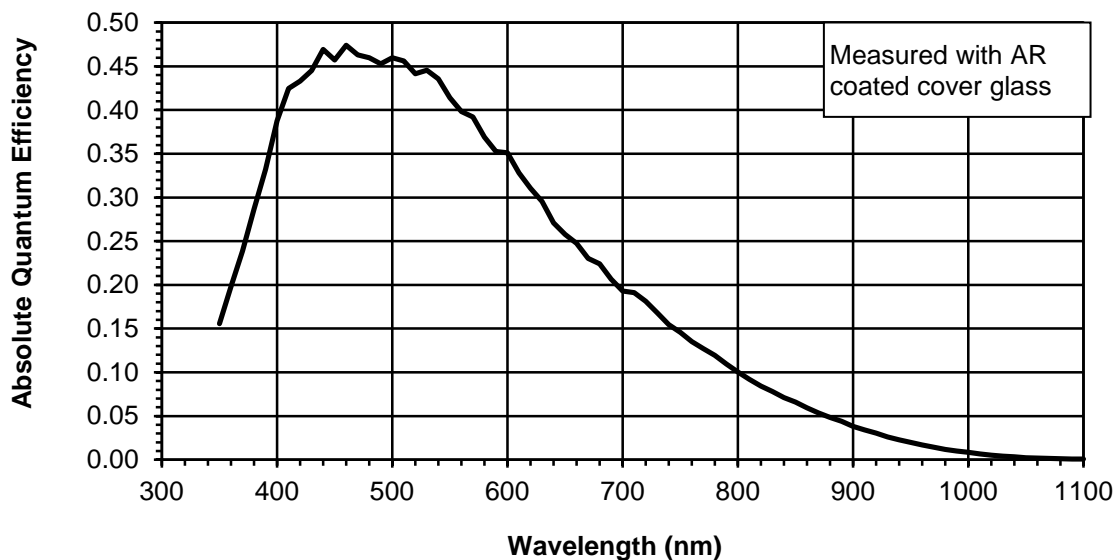


Figure 3: Monochrome with Microlens Quantum Efficiency

### MONOCHROME WITHOUT MICROLENS QUANTUM EFFICIENCY

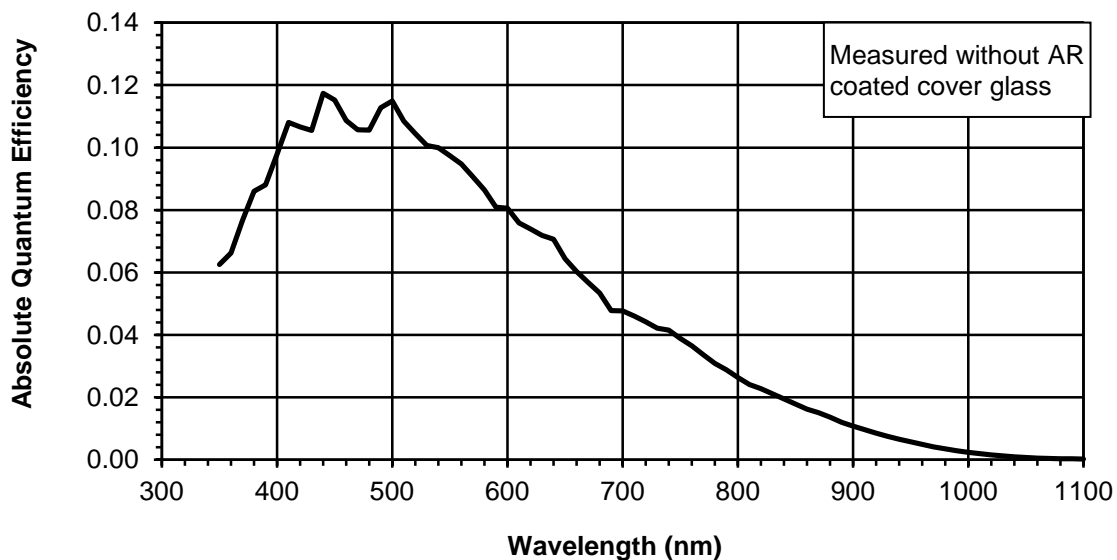


Figure 4: Monochrome without Microlens Quantum Efficiency



### COLOR WITH MICROLENS QUANTUM EFFICIENCY

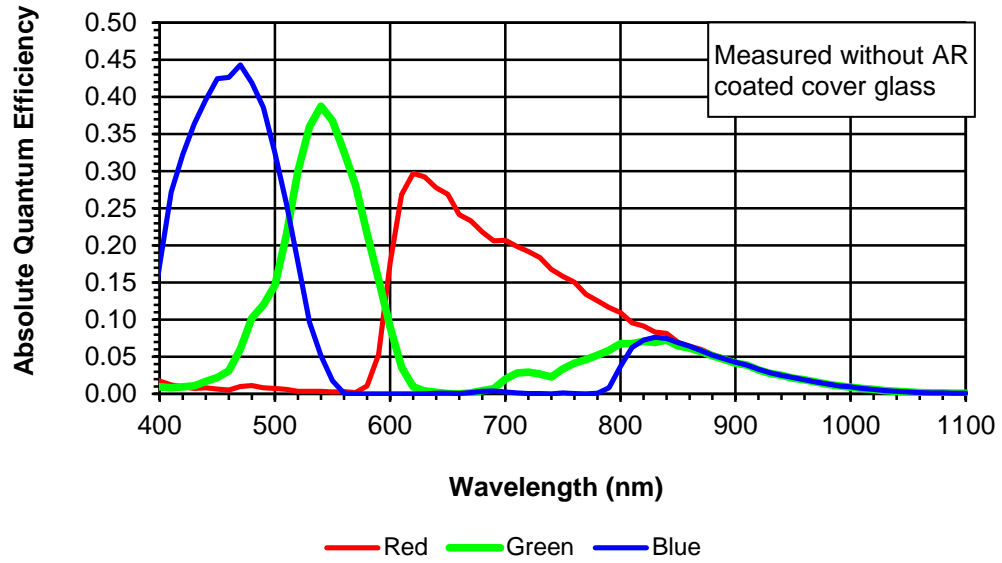


Figure 5: Color with Microlens Quantum Efficiency



### ANGULAR QUANTUM EFFICIENCY

For the curves marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

### Monochrome with Microlens

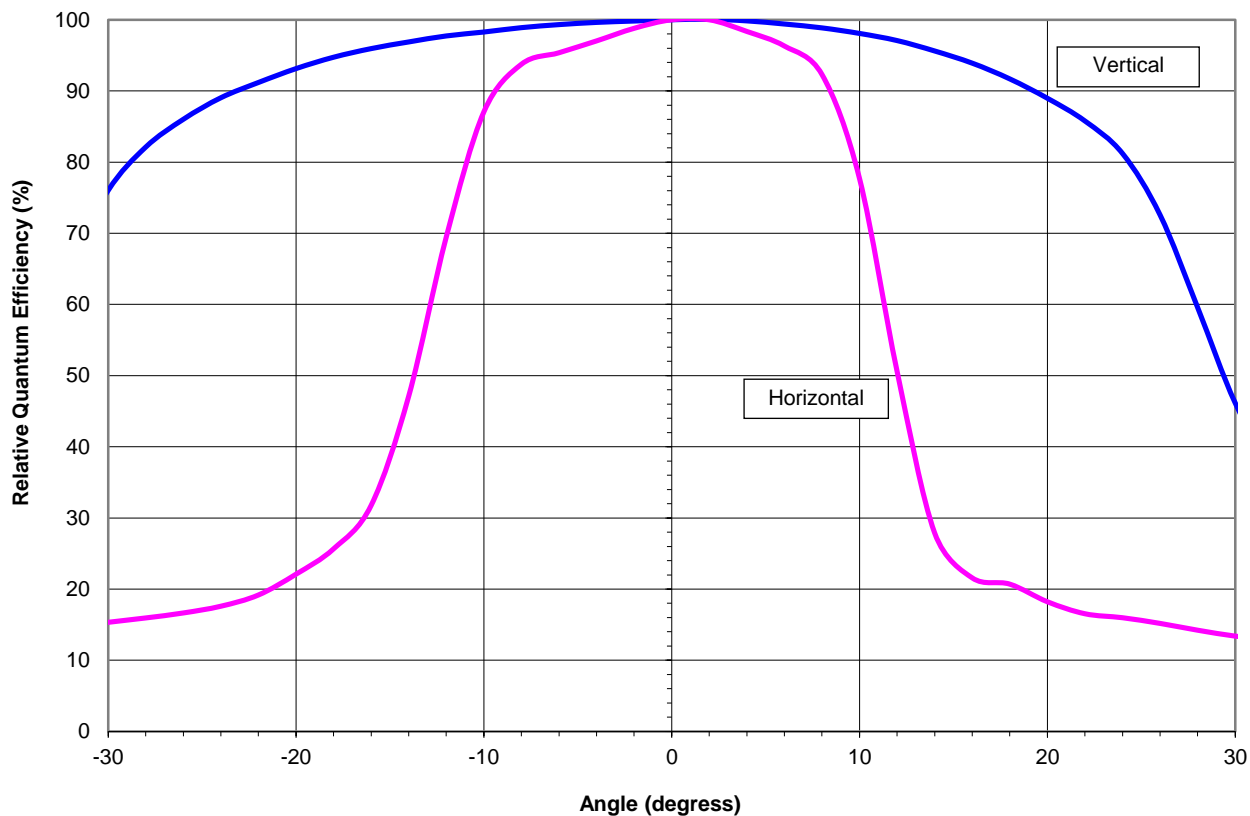


Figure 6: Monochrome with Microlens Angular Quantum Efficiency



## Defect Definitions

### OPERATIONAL CONDITIONS

All defect tests performed at  $t_{int} = t_{frame} = 908$  msec

### SPECIFICATIONS

Description	Definition	Class X Monochrome with Microlens Only	Class 1	Class 2 Monochrome	Class 2 Color	Notes
Major dark field defective bright pixel	Defect $\geq 245$ mV	150	150	300	300	2
Major bright field defective dark pixel	Defect $\geq 15\%$					
Minor dark field defective bright pixel	Defect $\geq 126$ mV	1500	1500	3000	3000	3
Cluster defect	A group of 2 to "N" contiguous major defective pixels, but no more than "W" adjacent defects horizontally	0	30 N=20 W=4	30 N=20 W=4	30 N=20 W=4	1, 2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	0	4	15	1, 2

#### Notes:

1. Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).
2. Tested at 27 °C and 40 °C.
3. Tested at 40 °C.

Class X sensors are offered strictly "as available". Truesense Imaging cannot guarantee delivery dates. Please call for availability.

### Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27 °C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps.



## Test Definitions

### TEST REGIONS OF INTEREST

Active Area ROI: Pixel (1, 1) to Pixel (4872, 3248)

Only the active pixels are used for performance and defect tests.

### OVERCLOCKING

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 7 for a pictorial representation of the regions.

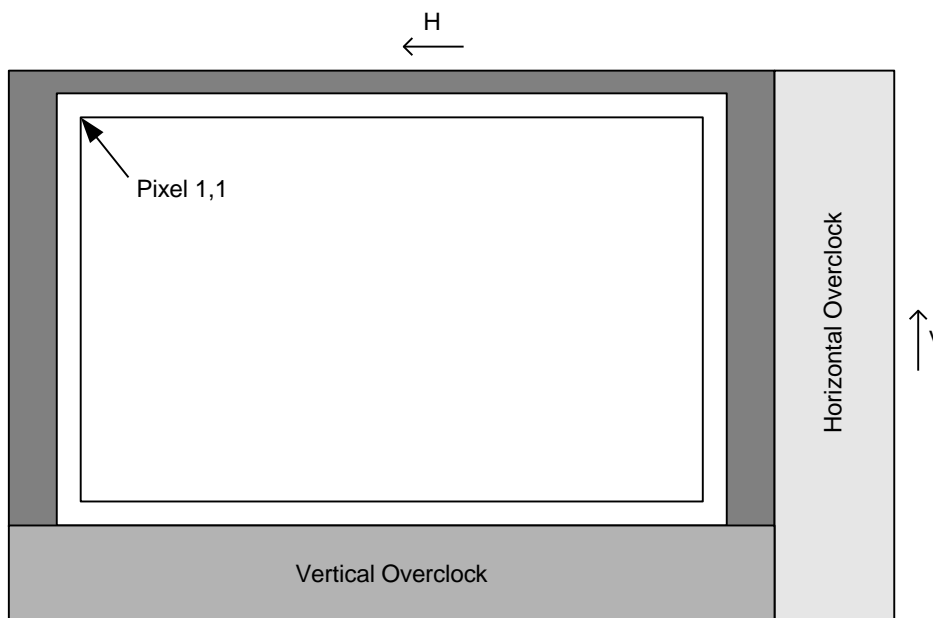


Figure 7: Overclock Regions of Interest



## TESTS

### Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 630 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 900 mV. Global non-uniformity is defined as

$$\text{Global Non - Uniformity} = 100 * \left( \frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right) \quad \text{Units: \%rms}$$

Active Area Signal = Active Area Average – Horizontal Overclock Average

### Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 384 sub regions of interest, each of which is 203 by 203 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

### Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 630mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 900mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal \* threshold

Bright defect threshold = Active Area Signal \* threshold

The sensor is then partitioned into 384 sub regions of interest, each of which is 203 by 203 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 630 mV
- Dark defect threshold:           630mV \* 15% = 95 mV
- Bright defect threshold:       630mV \* 15% = 95 mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 203, 203.
  - Median of this region of interest is found to be 630 mV.
  - Any pixel in this region of interest that is  $\geq (630+95 \text{ mV})$  725 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is  $\leq (630-95 \text{ mV})$  535 mV in intensity will be marked defective.
- All remaining 384 sub regions of interest are analyzed for defective pixels in the same manner.





## Operation

### ABSOLUTE MAXIMUM RATINGS

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T <sub>OP</sub>	-50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	I <sub>out</sub>	0.0	-40	mA	3
Off-chip Load	C <sub>L</sub>		10	pF	

Notes:

- Noise performance will degrade at higher temperatures.
- T=25 °C. Excessive humidity will degrade MTTF.
- Total for both outputs. Current is -20 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.

### MAXIMUM VOLTAGE RATINGS BETWEEN PINS

Description	Minimum	Maximum	Units	Notes
RL, RR, H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2SR, HLASTL, HLASTR to ESD	0	17	V	
Pin to Pin with ESD Protection	-17	17	V	1
VDDL, VDDR to GND	0	25	V	

Notes:

- Pins with ESD protection are: RL, RR, H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2SR, HLASTL, and HLASTR

### POWER UP SEQUENCE

- Substrate
- ESD Protection Disable
- All other clocks and biases



## DC BIAS OPERATING CONDITIONS

Description	Symbol	Pins	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	RDL, RDR	+11.5	+12.0	+12.0	V		
Output Amplifier Supply	VDD	VDDL, VDDR	+14.5	+15.0	+15.5	V		4
Ground	GND	GND	0.0	0.0	0.0	V		
Substrate	SUB	SUB	+8.0	VAB	+16.0	V		1, 5
ESD Protection Disable	ESD	ESD	-9.25	-9.0	-8.75	V		2
Output Bias Current	Iout	VOU TL, VOU TR		-5.0	-10.0	mA		3

### Notes:

- The operating of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of Vab is set such that the photodiode charge capacity is 30,000 electrons.
- VESD must be at least 1 V more negative than H1\_lo and H2\_lo during sensor operation AND during camera power turn on.
- An output load sink must be applied to Vout to activate output amplifier.
- The maximum DC current is for one output unloaded. This is the maximum current that the first two stages of one output amplifier will draw. This value is with Vout disconnected.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

## AC OPERATING CONDITIONS

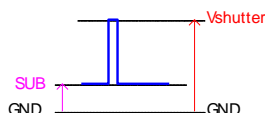
### Clock Levels

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V1, V3, V5, V7, V9, V11	V_2hi	+8.5	+9.0	+9.5	V	
Vertical CCD Clocks Midlevel	V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12	V_1mid, V_2mid	-0.2	0.0	+0.2	V	
Vertical CCD Clocks Low	V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12	V_1lo, V_2lo	-9.5	-9.0	-8.5	V	
Horizontal CCD Clocks Amplitude	H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2SR	H_amp	+4.5	+5.0	+5.5	V	
Horizontal CCD Clocks Low	H1SL, H1BL, H2SL, H2BL, H1SR, H1BR, H2SR, H2SR	H_lo	-5.0	-4.5	-4.0	V	
Horizontal Last CCD Amplitude	HLASTL, HLA STR	HLAST_amp	+4.5	+5.0	+5.5	V	
Horizontal Last CCD Low	HLASTL, HLA STR	HLAST_lo	-5.0	-4.5	-4.0	V	
Reset Clock Amplitude	RESETL, RESE TR	R_amp	+4.5	+5.0	+5.5	V	
Reset Clock Low	RESETL, RESE TR	R_lo	-3.5	-3.0	-2.5	V	
Electronic Shutter Voltage	SUB	Vshutter	+44	+48	+52	V	1
Fast Dump High	FDL, FDR	FD_hi	+4.5	+5.0	+5.5	V	
Fast Dump Low	FDL, FDR	FD_lo	-9.5	-9.0	-8.5	V	

### Notes:

- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

The figure below shows the DC bias (SUB) and AC clock (Vshutter) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.





## Clock Line Capacitances

Clocks	Capacitance	Units	Notes
Vertical CCD Phase 1 to GND	108	nF	1, 3
Vertical CCD Phase 2 to GND	118	nF	1, 4
Vertical CCD Phase 1 to Vertical CCD Phase 2	56	nF	3, 4
H1S to GND	27	pF	2
H2S to GND	27	pF	2
H1B to GND	13	pF	2
H2B to GND	4	pF	2
H1S to H2B and H2S	13	pF	2
H1B to H2B and H2S	13	pF	2
H2S to H1B and H1S	13	pF	2
H2B to H1B and H1S	13	pF	2
HLAST to GND	20	pF	2
RESET to GND	10	pF	
FD to GND	20	pF	

### Notes:

1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, these values are for half of the imager (H1SL, H1BL, H2SL, H2BL and H1BINL or H1SR, H1BR, H2SR, H2BR and H1BINR).
3. Vertical CCD Phase 1: V2, V4, V6, V8, V10, V12
4. Vertical CCD Phase 2: V1, V3, V5, V7, V9, V11



## Timing

### REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
VCCD to HCCD Delay	$T_{HD}$	4	6		$\mu\text{s}$	
VCCD Transfer Time	$T_{VCCD}$	4	6		$\mu\text{s}$	
HCCD to VCCD Delay	$T_{HL}$		50		ns	
Photodiode transfer time	$T_{V3rd}$	10	12		$\mu\text{s}$	
VCCD Pedestal time	$T_{3P}$	200	600		$\mu\text{s}$	
VCCD Delay	$T_{3D}$	12	20		$\mu\text{s}$	
VCCD Delay Before Pedestal	$T_{DEL}$		50		ns	
VCCD Delay Before 1st Line	$T_{D1L}$	10	60		$\mu\text{s}$	
Reset Pulse time	$T_R$		3.25		ns	
VCCD to HCCD Delay – Shutter	$T_{HDS}$		6		$\mu\text{s}$	
Shutter Pulse time	$T_S$		4		$\mu\text{s}$	
Shutter Pulse delay	$T_{SD}$		1.5		$\mu\text{s}$	
HCCD Clock Period	$T_H$	33.3			ns	
VCCD rise/fall time	$T_{VR}$	0.2			$\mu\text{s}$	
Fast Dump Gate Leading Delay	$T_{FDL}$	0.5			$\mu\text{s}$	
Fast Dump Gate Trailing Delay	$T_{FDT}$	0.5			$\mu\text{s}$	
VCCD Line Clock Leading Edge Delay	$T_{VL}$	0.2	0.3	0.4	$\mu\text{s}$	
VCCD Line Clock Trailing Edge Delay	$T_{VT}$	0.0	0.2	0.4	$\mu\text{s}$	

### MAIN TIMING – CONTINUOUS MODE

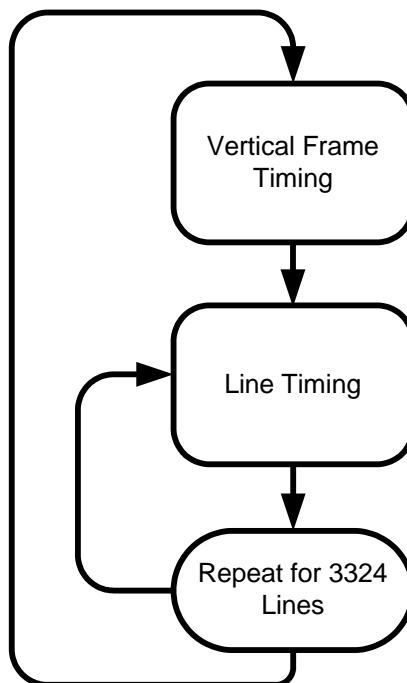


Figure 8: Main Timing - Continuous Mode



### FRAME TIMING – CONTINUOUS MODE

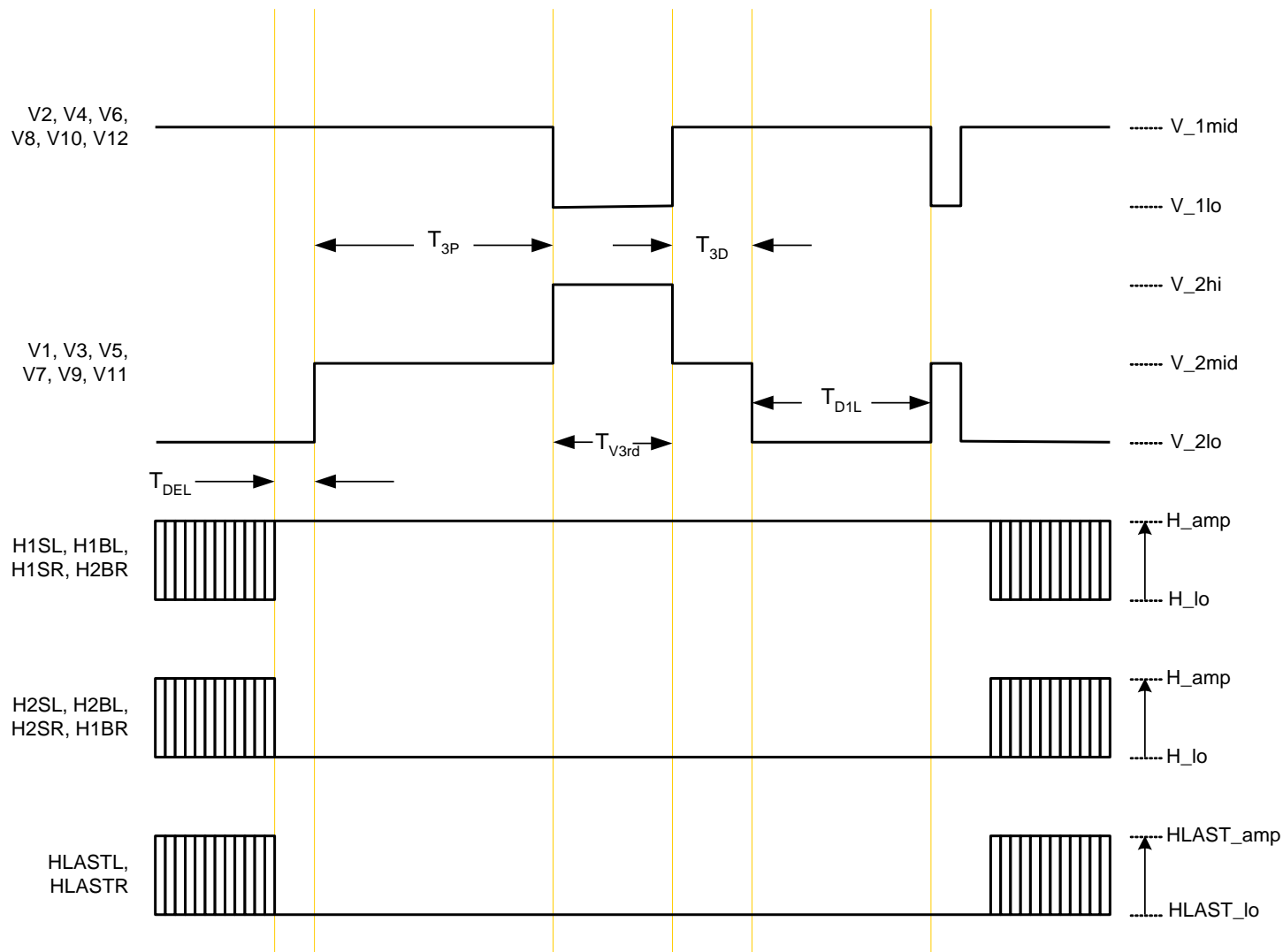


Figure 9: Framing Timing



## LINE TIMING CONTINUOUS MODE

### Line Timing Single Output

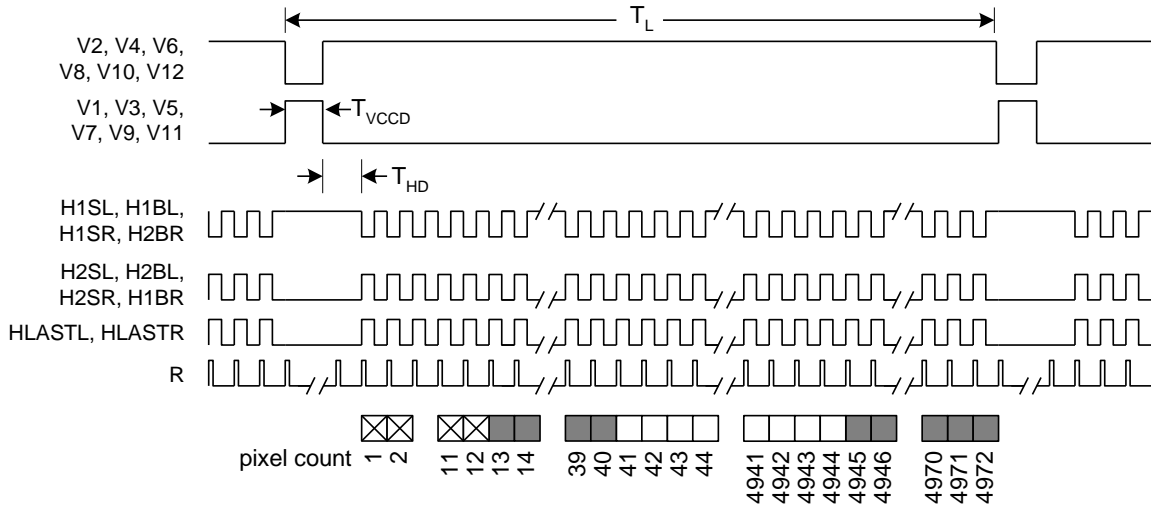


Figure 10: Line Timing Single Output

### Line Timing Double Output

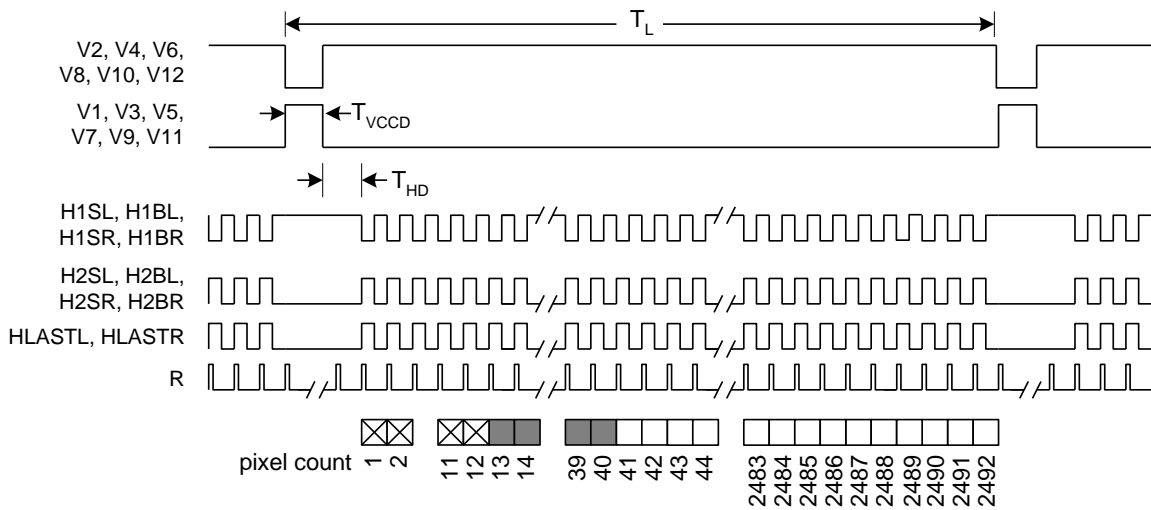


Figure 11: Line Timing Dual Output



### Line Timing Detail Single Output

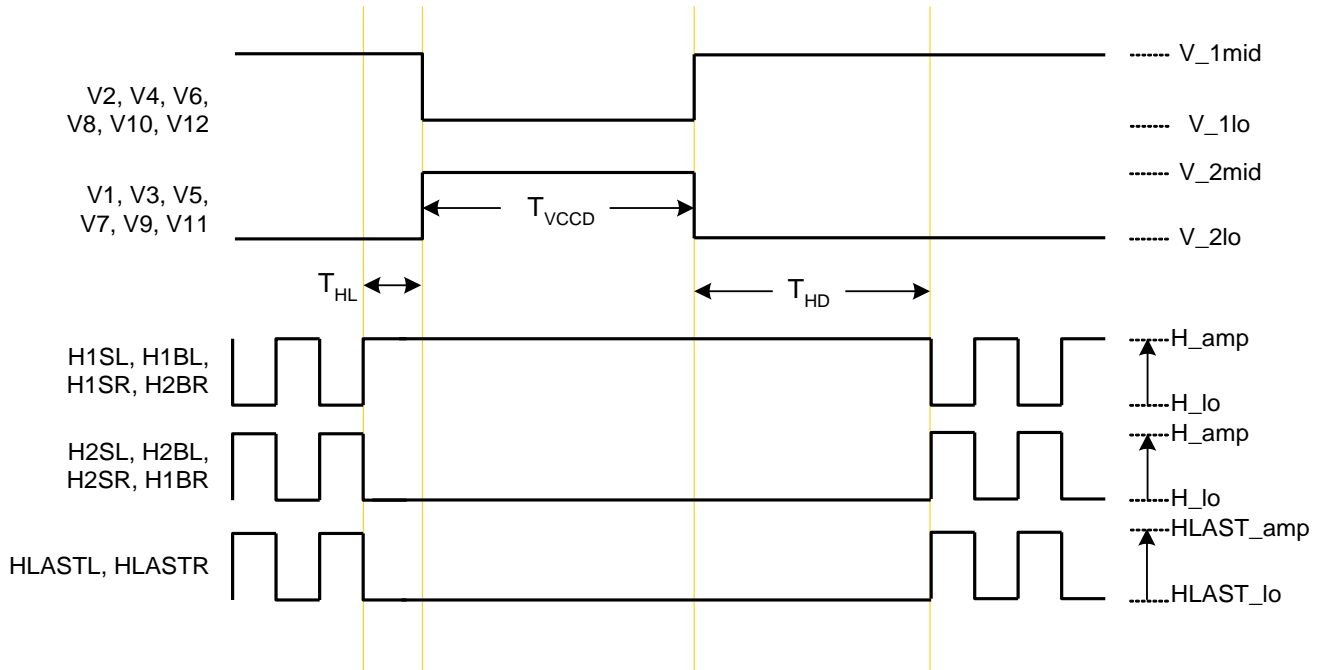


Figure 12: Line Timing Detail Single Output

### Line Timing Detail Edge Alignment

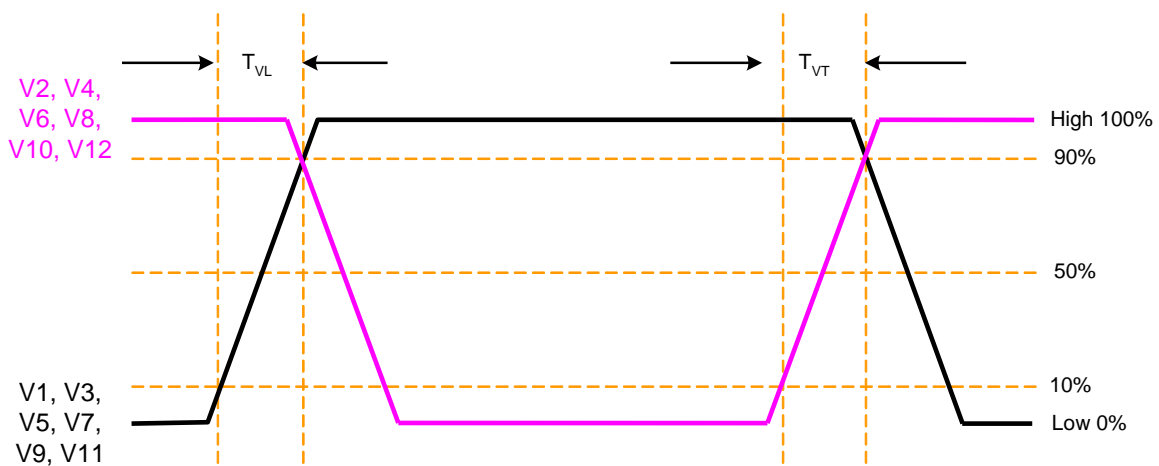


Figure 13: Line Timing Detail Edge Alignment



### PIXEL TIMING

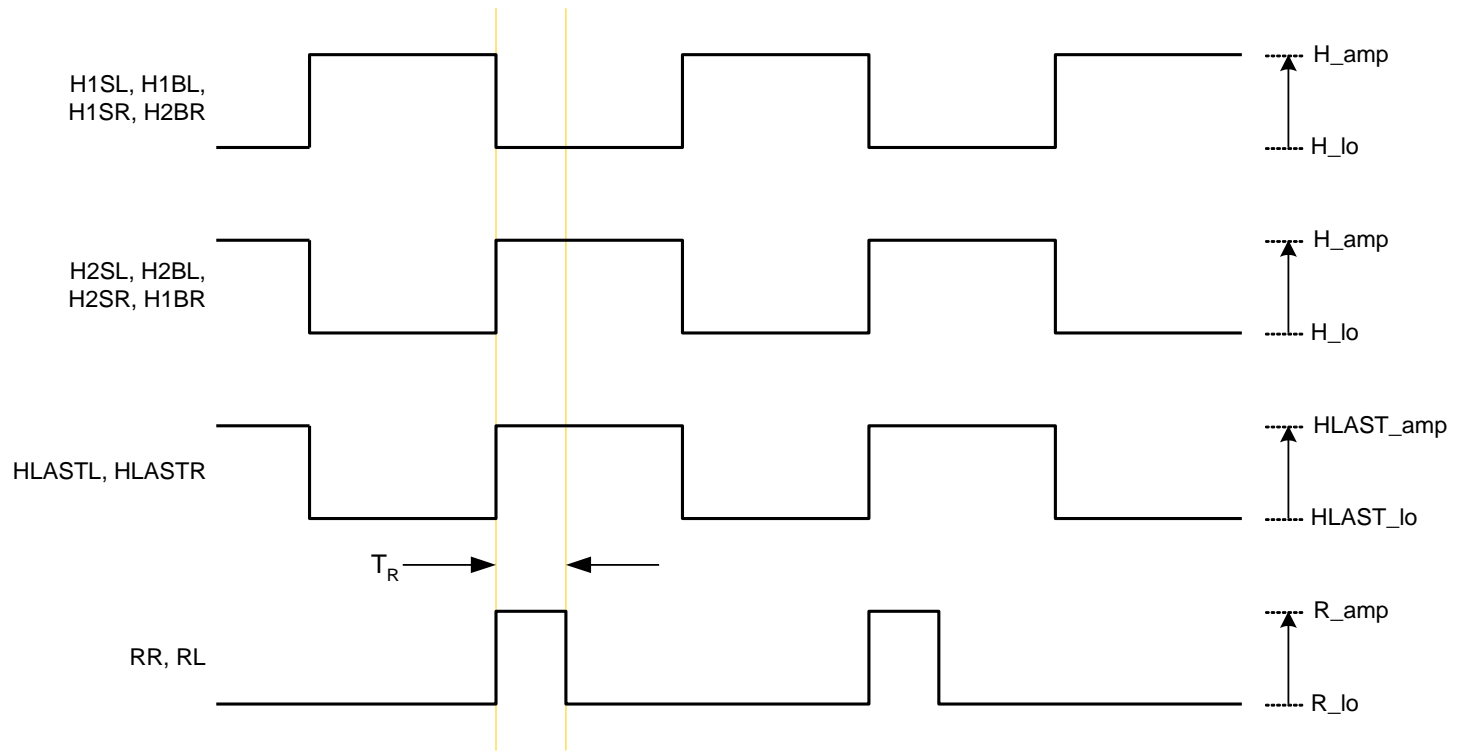


Figure 14: Pixel Timing





### FAST LINE DUMP TIMING

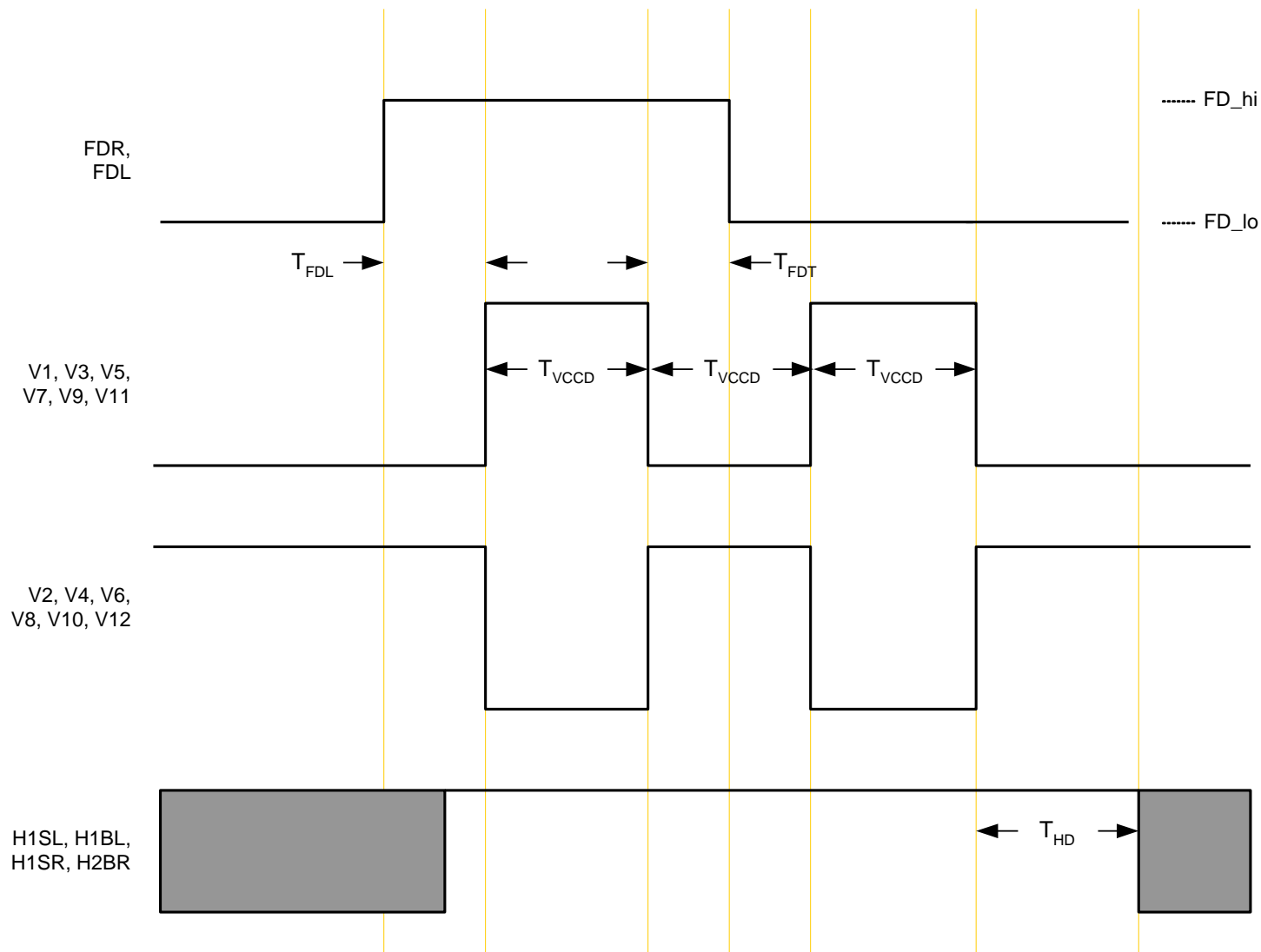


Figure 15: Fast Line Dump Timing



### ELECTRONIC SHUTTER TIMING

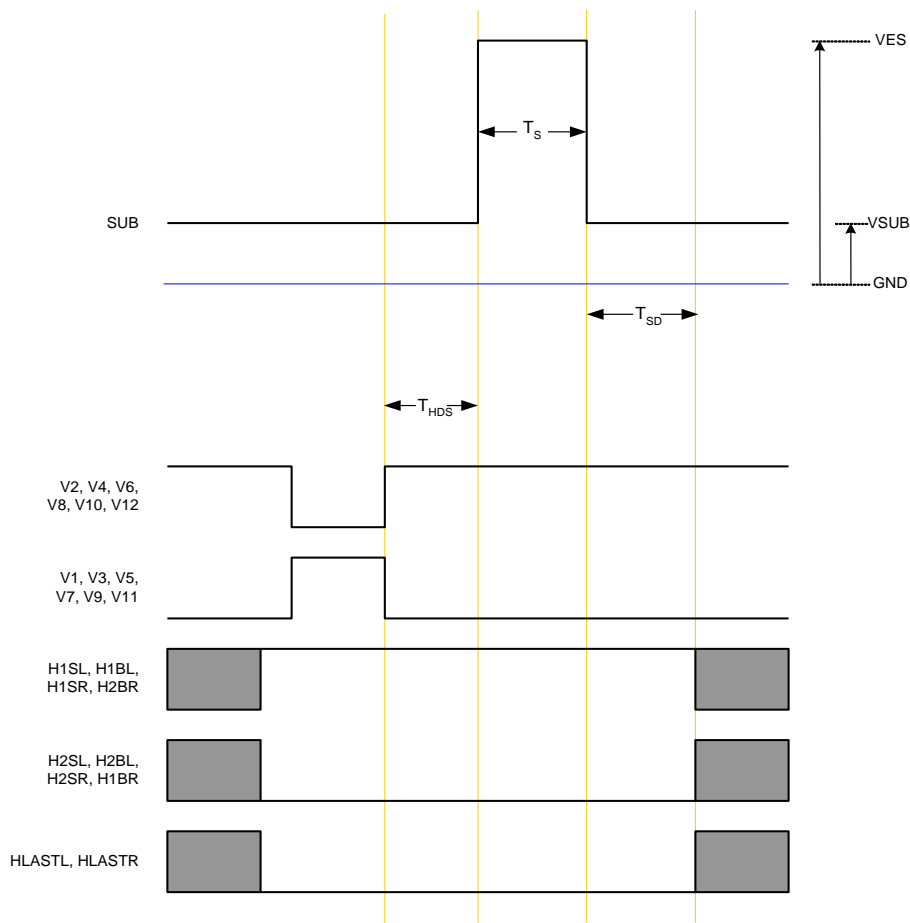


Figure 16: Electronic Shutter Timing

### ELECTRONIC SHUTTER INTEGRATION TIME DEFINITION

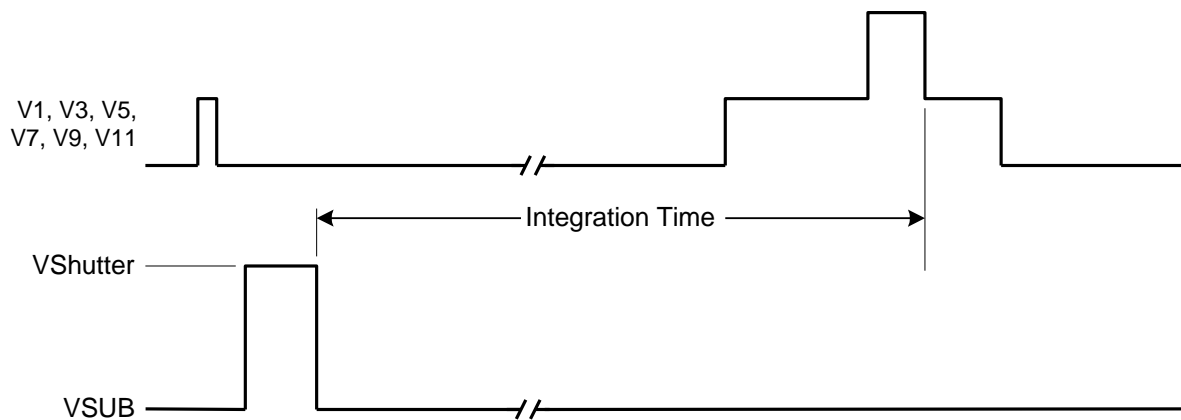


Figure 17: Integration Time Definition



## Storage and Handling

### STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Temperature	T	-55	80	°C	1
Humidity	RH	5	90	%	2

#### Notes:

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTF.

### ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

### COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

### ENVIRONMENTAL EXPOSURE

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

### SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.



## Mechanical Drawings

### COMPLETED ASSEMBLY

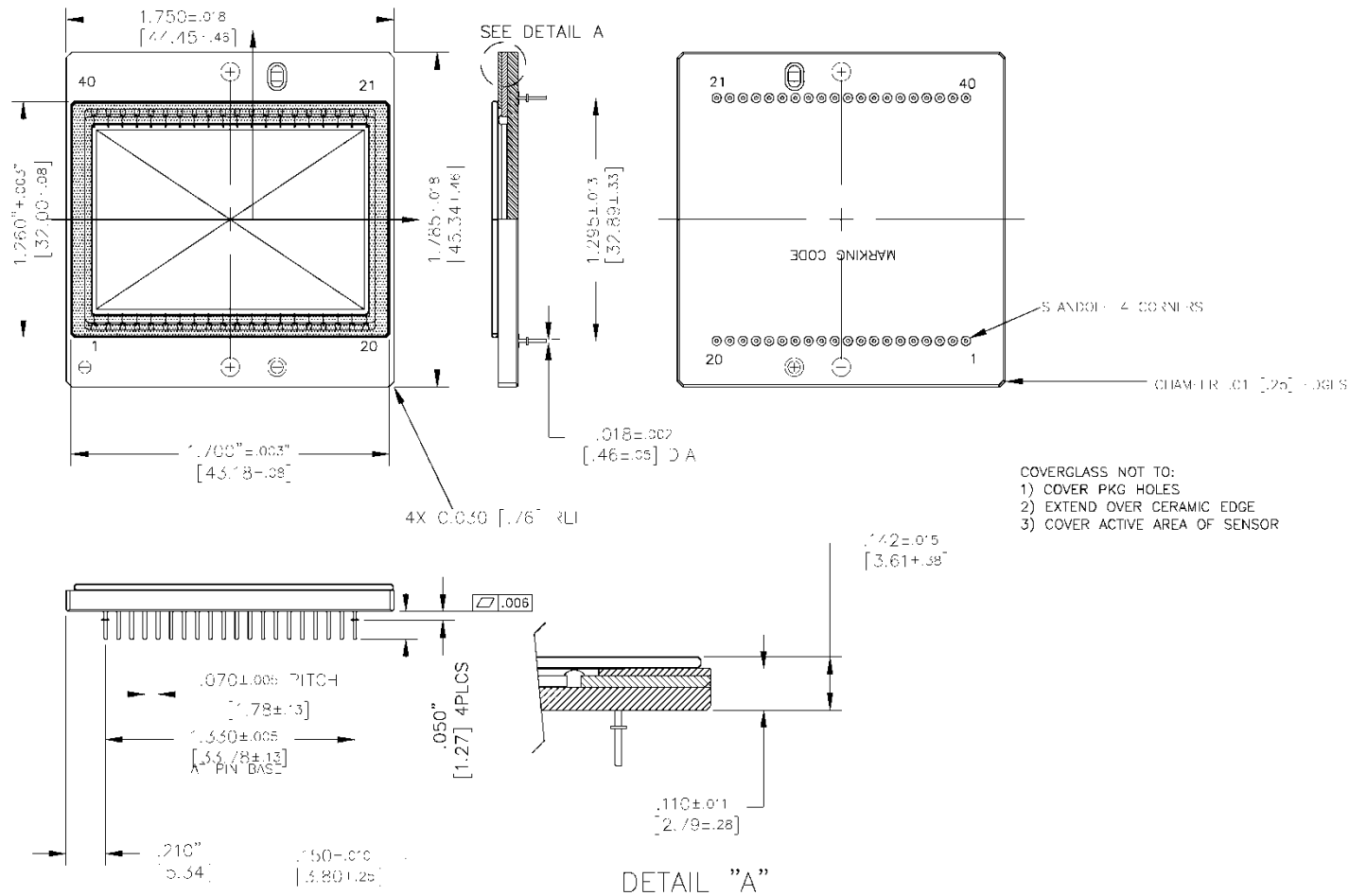


Figure 18: Completed Assembly (1 of 2)

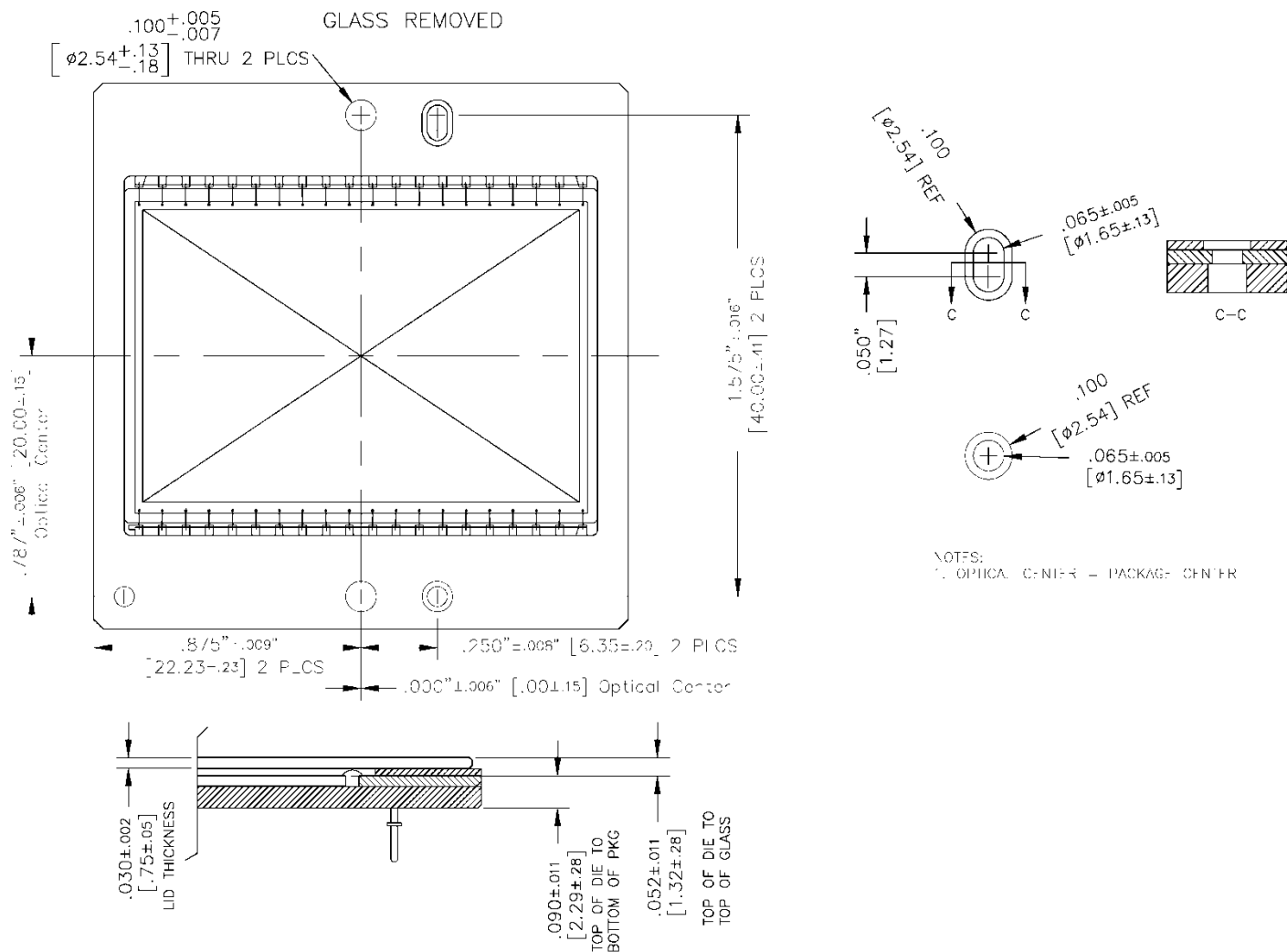
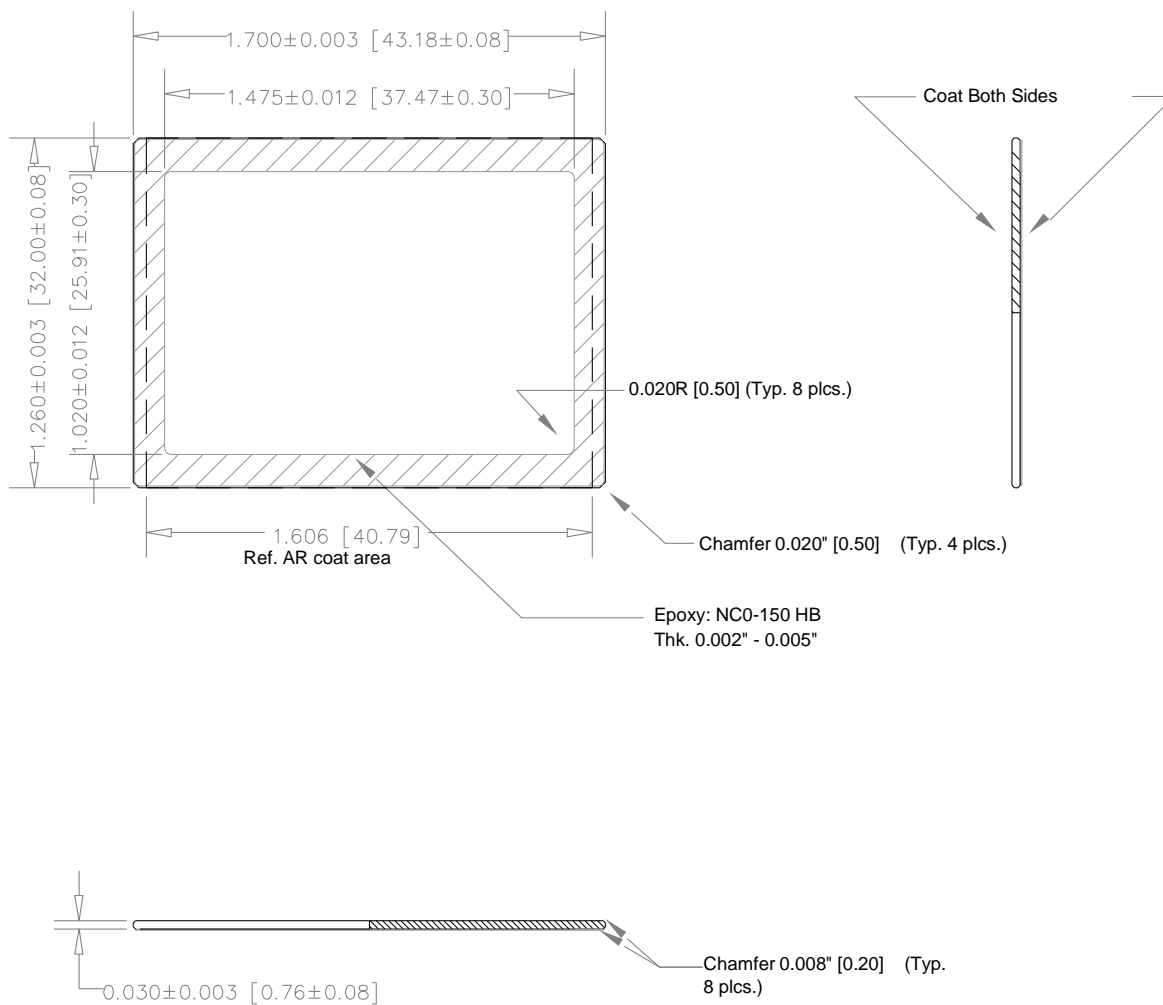


Figure 19: Completed Assembly (2 of 2)



### COVER GLASS



**NOTES:**

1. Multi-Layer Anti-Reflective Coating on 2 sides:  
 Double Sided Reflectance:  
 Range (nm)  
 420 - 450 nm < 2%  
 450 - 630 nm < 1%  
 630 - 680 nm < 2%
2. Dust, Scratch specification - 20 microns max.
3. Substrate - Schott D263T eco or Equivalent
4. Epoxy: NCO-150HB  
 Thickness: 0.002" - 0.005"

Figure 20: Glass Drawing



### GLASS TRANSMISSION

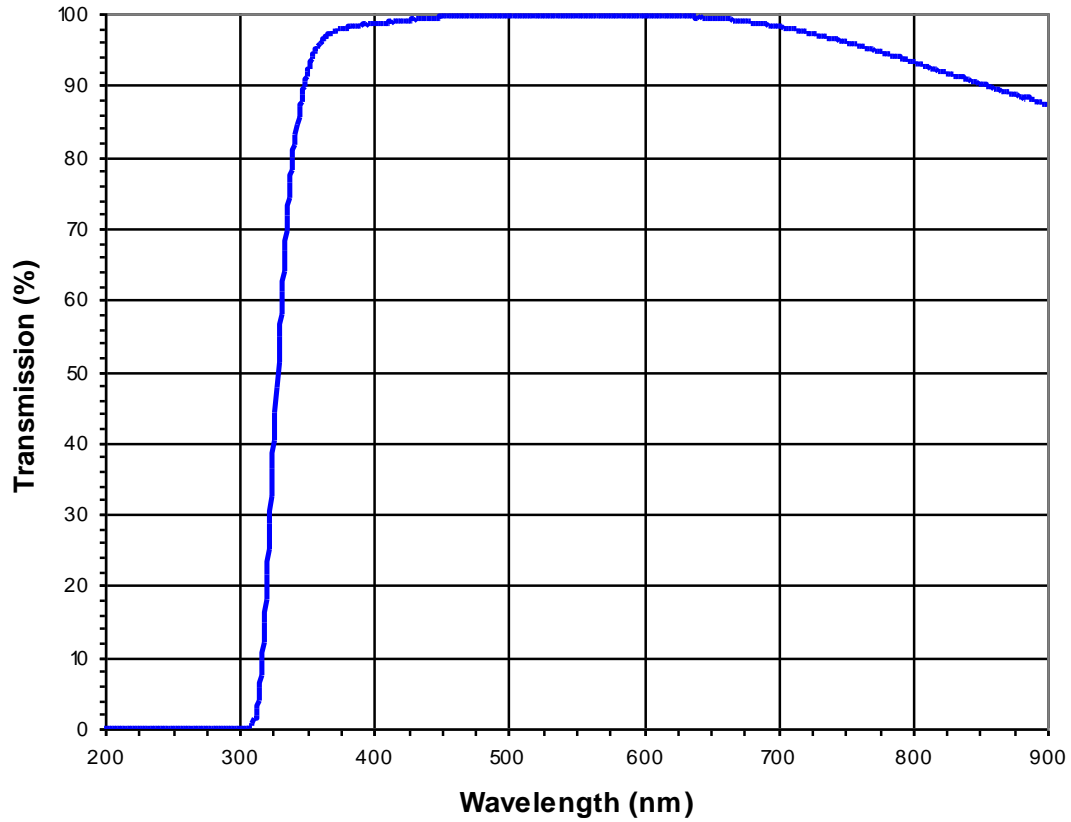


Figure 21: Glass Transmission



## Quality Assurance and Reliability

### QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

### REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

### LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

### LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

### TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

### MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

## Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.





## Revision Changes

### MTD/PS-1027

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> <li>Initial release</li> </ul>
2.0	<ul style="list-style-type: none"> <li>Added Monochrome Sealed Cover Glass Part Numbers to the Ordering Information page.</li> </ul>
3.0	<ul style="list-style-type: none"> <li>Added reference to Website for acquiring related documentation</li> <li>Corrected number of dummy pixels. Changed from 13 dummy pixels to 12 dummy pixels.</li> <li>Clock Line Capacitances, corrected Note 4 from Vertical CCD Clock Phase 1 to Vertical CCD Clock Phase 2</li> <li>Corrected number of dummy pixels in Line Timing figures. Changed from 13 dummy pixels to 12 dummy pixels.</li> <li>Line Timing Edge Alignment – updated vertical CCD clock designations</li> <li>Fast Line Dump Timing – updated vertical CCD clock designations</li> <li>Electronic Shutter Integration Time Definition – updated vertical CCD clock designation</li> <li>Storage and Handling Section               <ul style="list-style-type: none"> <li>Updated item 3 in ESD section</li> <li>Updated item 3 in Cover Glass Care and Cleanliness section</li> </ul> </li> </ul>
4.0	<ul style="list-style-type: none"> <li>Added Monochrome, Microlens, Taped Cover Glass Part Numbers to the Ordering Information page.</li> </ul>
5.0	<ul style="list-style-type: none"> <li>Corrected Reset Low nominal and minimum values. The values were swapped.</li> <li>Added the note “Refer to Application Note <i>Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions</i>” to the following sections               <ul style="list-style-type: none"> <li>DC Bias Operating Conditions</li> <li>AC Operating Conditions</li> <li>Storage and Handling</li> </ul> </li> <li>Changed cover glass material to D263T eco or equivalent</li> </ul>
6.0	<ul style="list-style-type: none"> <li>Added Monochrome, Microlens, Sealed MAR cover glass Class X part number to Ordering Information table</li> <li>Added Monochrome, Microlens, Sealed MAR cover glass Class X defect definition to the Defect Definitions table</li> </ul>

### PS-0013

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> <li>Initial release with new document number, updated branding and document template</li> <li>Updated <i>Storage and Handling</i> and <i>Quality Assurance and Reliability</i> sections</li> </ul>
2.0	<ul style="list-style-type: none"> <li>The completed assembly drawing was updated to clarify the placement of the sensor in the package. The location of the sensor in the package has not changed. The drawing was updated only to clarify the sensor location.</li> </ul>
3.0	<ul style="list-style-type: none"> <li>Corrected Top of Die to Bottom of Package dimension from 0.025 to 0.090 in Completed Assembly drawing</li> </ul>
3.1	<ul style="list-style-type: none"> <li>Updated branding</li> </ul>

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